PHYS225
Lecture 8
Electronic Circuits
• In the schematic above (emitter follower), $V_{\text{out}} = V_{\text{in}} - 0.6$
  - sounds useless, right?
  - there is no voltage “gain,” but there is current gain
  - Imagine we change $V_{\text{in}}$ by $\Delta V$: $V_{\text{out}}$ changes by the same $\Delta V$
  - so the transistor current changes by $\Delta I_e = \Delta V/R$
  - but the base current changes $1/\beta$ times this (much less)
  - so the “signal in” thinks the load is $\Delta V/\Delta I_b = \beta \cdot \Delta V/\Delta I_e = \beta R$
  - the load is very high
• The “buffer” is a way to drive a load without the driver feeling the pain (as much): it’s impedance isolation
Last lecture

– Field Effect Transistor
  • JFET
  • MOSFET

– Can be thought of as a “voltage controlled resistor”
  • Voltage on “gate” controls impedance between “source” and “drain”
  • No current flows into gate
    – Input impedance is very high

– There are n- and p-type FETs
  • As with BJT
Field-Effect Transistors

• The “standard” npn and pnp transistors use base-current to control the transistor current
• FETs use a field (voltage) to control current
• Result is no current flows into the control “gate”

<table>
<thead>
<tr>
<th>ON CHARACTERISTICS*</th>
<th>2N7000 FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{GS(th)}$</td>
<td>Gate Threshold Voltage</td>
</tr>
<tr>
<td>$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$</td>
<td>0.8, 2.1, 3, V</td>
</tr>
<tr>
<td>$R_{DS(ON)}$</td>
<td>Static Drain-Source On-Resistance</td>
</tr>
<tr>
<td>$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$</td>
<td>1.2, 5, Ω</td>
</tr>
<tr>
<td>$V_{DS(ON)}$</td>
<td>Drain-Source On-Voltage</td>
</tr>
<tr>
<td>$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$</td>
<td>0.6, 2.5, V</td>
</tr>
<tr>
<td>$V_{GS} = 4.5\text{ V}, I_D = 75\text{ mA}$</td>
<td>0.14, 0.4, V</td>
</tr>
<tr>
<td>$I_{D(ON)}$</td>
<td>On-State Drain Current</td>
</tr>
<tr>
<td>$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$</td>
<td>75, 600, mA</td>
</tr>
<tr>
<td>$g_{FS}$</td>
<td>Forward Transconductance</td>
</tr>
<tr>
<td>$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$</td>
<td>100, 320, ms</td>
</tr>
</tbody>
</table>
FET Generalities

• Every FET has at least three connections:
  – source (S)
    • Like emitter (E) on BJT
  – drain (D)
    • Like collector (C) on BJT
  – gate (G)
    • Like base (B) on BJT

• Some have a body connection too
  – though often tied to source
FET Types

- Two flavors: n and p
- Two types: JFET, MOSFET
- MOSFETs more common
- JFETs conduct “by default”
  - when $V_{\text{gate}} = V_{\text{source}}$
- MOSFETs are “open” by default
  - must turn on deliberately
- JFETs have a p-n junction at the gate, so must not forward bias more than 0.6 V
- MOSFETs have total isolation: do what you want
JFET Switch

• An ideal switch would make a short-circuit connection when “on” and an open connection when “off.” In other words, it would behave like a mechanical switch.

• The following switch quenches current flow when the JFET gate is reverse-biased below the cutoff level.
JFET Switch

On state = signal passed $\Rightarrow R_{DS} \approx 25 - 100\Omega$
Off state = open circuit $\Rightarrow R_{DS} \approx 10\ G\Omega$

- $V_{out}=V_{in}$ when switch is “on”
- $V_{out}=0$ when switch is “off”
- Circuit behaves like a voltage divider when on.

$$v_{out} = \frac{v_{in}R_1}{R_1 + R_{JFET}}$$

$R_1 \gg R_{JFET}$

$$v_{out} \approx v_{in}$$

$R_1 \ll R_{JFET}$

$$v_{out} \approx 0$$
FET Switch Operates in Linear Regime

- Switch “off” corresponds to $V_{GS} = V_{GS(\text{off})}$.
- Switch “on” corresponds to $V_{GS} > V_{GS(\text{off})}$.
- Ideally, RFET is small, i.e. IV slope is large below.
CMOS Switch

- Complementary MOSFET (CMOS) switch is most common.
- With this circuit, the output swing spans the full range.
- Note the absence of resistors; power is low.
- Q1 and Q2 are not “on” at same time -> no current!
Source Follower

- A “source follower” circuit uses a FET in a circuit in which $v_s$ “follows” $v_g$.
- It converts the output impedance of a signal from high to low. This is useful for driving long cables with small signals.

\[
\begin{align*}
    v_s &= R_i d \\
    i_d &= g_m v_{gs} = g_m(v_g - v_s) \\
    v_s &= [R_g m/(1+R_g m)]v_g \\
    \text{gain} &= \frac{v_s}{v_g} = 1/(1+1/R_g m) \\
\end{align*}
\]

So, gain~1 for $R_g m >> 1$.

Note that $g_m$ is the transconductance, and $1/g_m$ is the output impedance, typically ~a few hundred Ohms.

By replacing the resistor with a current source, $R \sim \infty$, so gain is nearer to 1.
Source Follower with Current Source

- By replacing the resistor with a current source, $R \approx \infty$, so gain is nearer to 1.
- The current source is made of a FET with grounded gate.
FET Current Source: Schematic

- A self-biased FET will deliver a nearly fixed current regardless of load if operated in the saturation region.
FET Current Source: Biasing

- The current source is most stable at $V_{GS}$ just above the cutoff voltage ($V_{GS,off}$).
- This is where the transconductance goes to zero.

**Basic Source Biasing**

For a given device where $I_{DSS}$ and $V_{GS(off)}$ are known, the approximate $V_{GS}$ required for a given $I_D$ is

$$V_{GS} = V_{GS(off)} \left[ 1 - \left( \frac{I_D}{I_{DSS}} \right)^{1/k} \right]$$

(1)

where $k$ can vary from 1.8 to 2.0, depending on device geometry. If $K = 2.0$, the series resistor $R_S$ required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad \text{or} \quad R_S = \frac{V_{GS(off)}}{I_D} \left( 1 - \sqrt{\frac{I_D}{I_{DSS}}} \right)$$

(2)

A change in supply voltage or a change in load impedance, will change $I_D$ by only a small factor because of the low output conductance $g_{oss}$.

$$\Delta I_D = (\Delta V_{DS})(g_{oss})$$

(3)

The value of $g_{oss}$ is an important consideration in the accuracy of a constant-current source where the supply voltage may vary. As $g_{oss}$ may range from less than 1 µS to more than 50 µS according to the FET type, the dynamic impedance can be greater than 1 MΩ to less than 20 kΩ. This corresponds to a current stability range of 1 µA to 50 µA per volt. The value of $g_{oss}$ also depends on the operating point. Output conductance $g_{oss}$ decrease approximately linearly with $I_D$. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}}$$

(4)

where $g_{oss} = g'_{oss}$

(5)

when $V_{GS} = 0$

(6)

So as $V_{GS} \to V_{GS(off)}$, $g_{oss} \to$ Zero. For best regulation, $I_D$ must be considerably less than $I_{DSS}$. 

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FET Current Source: Parts

• The following table gives output current versus bias resistance for a variety of parts.

Choosing the Correct JFET for Source Biasing

Each of the Siliconix device data sheets include typical transfer curves that can be used as illustrated in Figure 7.

Several popular devices are ideal for source biased current sources covering a few μAs to 20 mA. To aid the designer, the devices in Table 1 have been plotted to show the drain current, $I_D$, versus the source resistance, $R_S$, in Figures 8, 9, and 10. Most plots include the likely worst case $I_D$ variations for a particular $R_S$. For tighter current control, the JFET production lot can be divided into ranges with an appropriate resistor selection for each range.

<table>
<thead>
<tr>
<th>Practical Current Range $I_D$ (mA)</th>
<th>Through-Hole Plastic Device</th>
<th>Surface Mount Device</th>
<th>Metal Can Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01 – 0.02</td>
<td>PN4117A</td>
<td>SST4117</td>
<td>2N4117A</td>
</tr>
<tr>
<td>0.01 – 0.04</td>
<td>PN4118A</td>
<td>SST4118</td>
<td>2N4118A</td>
</tr>
<tr>
<td>0.02 – 0.1</td>
<td>PN4119A</td>
<td>SST4119</td>
<td>2N4119A</td>
</tr>
<tr>
<td>0.01 – 0.1</td>
<td>J201</td>
<td>SST201</td>
<td>2N4338</td>
</tr>
<tr>
<td>0.04 – 0.8</td>
<td>J202</td>
<td>SST202</td>
<td>2N4339</td>
</tr>
<tr>
<td>0.1 – 2</td>
<td>J113</td>
<td>SST113</td>
<td>2N4393</td>
</tr>
<tr>
<td>0.2 – 10</td>
<td>J112</td>
<td>SST112</td>
<td>2N4392</td>
</tr>
</tbody>
</table>

Figure 10. JFET Source Biased Drain-Current vs. Source Resistance
MOSFET Switches

- MOSFETs, as applied to logic designs, act as voltage-controlled switches
  - n-channel MOSFET is closed (conducts) when positive voltage (+5 V) is applied, open when zero voltage
  - p-channel MOSFET is open when positive voltage (+5 V) is applied, closed (conducts) when zero voltage

(MOSFET means metal-oxide semiconductor field effect transistor)
Power Transistors

- Additional material for current handling and heat dissipation
- Can handle high current and voltage
- Functionally the same as normal transistors